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10/586,846	07/20/2006	Ingrid Verbauwhede	UCLARF.004NP	3453
29995 7590 12/16/2009 KNOBBE MARTENS OLSON & BEAR LLP 2040 MAIN STREET FOURTEENTH FLOOR IRVINE, CA 92614				
EXAMINER				
TABLER, MATTHEW C				
ART UNIT		PAPER NUMBER		
2819				
NOTIFICATION DATE		DELIVERY MODE		
12/16/2009		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary

Application No.

10/586,846

Applicant(s)

VERBAUWHUDE ET AL.

Examiner

MATTHEW C. TABLER

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 November 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 3-12 and 23-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 3-12 and 23-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 July 2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB06)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ ~~Notes of Informal Patent Application~~
- 6) ☐ Other: _____

DETAILED ACTION

This office action is in response to applicant's remarks filed on November 12th, 2009. Currently, claims 3-12 and 23-26 are pending.

Drawings

- 1) The drawings are objected to because the handwriting is difficult to read.
- 2) The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "pre-discharged *logic cell*" in claim 4, the "differential dynamic logic register configured to *generate* a pre-charge wave" in claims 5-6, 10 and 12, and the "precharge generator" in claim 8 must be shown or the feature(s) canceled from the claim(s). In summary, the drawings do not show any circuit *generating* a precharge or predischARGE signal. (The drawings disclose a plurality of circuits *receiving* a precharge or predischARGE signal; no objection is made to claims 3, 9 and 11 for this reason.) No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 3-12 and 23-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Morzano (US Patent Application 2001/0046169) published on November 29th, 2001.

Regarding claim 3, Morzano shows a wave dynamic differential logic (Figure 2), comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs DI and DI*), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs N1 and P1), said differential logic cell configured to propagate a precharge wave and/or a predischarges wave (precharge/predischarge signal EN).

(The EN signal is activated to precharge and predischage the differential logic circuit; see the Abstract and description for Figure 2.)

Regarding claim 4, Morzano shows a wave dynamic differential logic, comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs DI and DI*), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs N1 and P1), and a pre-discharged logic cell configured to generate a pre-discharge wave to pre-discharge said differential logic cell and/or a precharged logic cell configured to generate a precharge wave to pre-charge said differential logic cell (EN signal precharges and predischages the differential logic circuit).

Regarding claim 5, Morzano shows a wave dynamic differential logic, comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs DI and DI*), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs N1 and P1), and a master-slave differential dynamic logic register configured to generate a pre-charge wave to pre-charge said differential logic cell (register comprises first stage comprising 38 and 39 and secondary stage 40 and 42, EN signal precharges and predischages the differential logic circuit).

Regarding claim 6, Morzano shows a wave dynamic differential logic, comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs DI and DI*), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic

outputs (outputs N1 and P1), and a master-slave differential dynamic logic register configured to generate a pre-discharge wave to pre-discharge said differential logic cell (register comprises first stage comprising 38 and 39 and secondary stage 40 and 42, EN signal precharges and predischarges the differential logic circuit).

Regarding claim 7, Morzano shows a wave dynamic differential logic DPA-resistant logic circuit (Figure 2), comprising a first logic tree configured to receive inverted inputs and corresponding non-inverted inputs (inputs DI and DI*) and to produce one or more first outputs (outputs N1 and P1), and a dual of said first logic tree configured to receive said inverted inputs and said corresponding non-inverted inputs and produce one or more inverted first outputs (outputs N1 and P1).

Regarding claim 8, Morzano shows a wave dynamic differential logic wherein a differential logic cell transmits a precharge value generated by a precharge generator (EN signal).

Regarding claim 9, Morzano shows a wave dynamic differential logic, comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs DI and DI*), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs N1 and P1), and a master-slave differential dynamic logic register configured to transmit on a pre-charge wave to pre-charge said differential logic cell (register comprises first stage comprising 38 and 39 and secondary stage 40 and 42, EN signal precharges and predischarges the differential logic circuit).

Regarding claim 10, Morzano shows a wave dynamic differential logic, comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs DI and DI*), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs N1 and P1), and a differential dynamic logic register configured to generate a pre-charge wave to pre-charge said differential logic cell (EN signal precharges and predischarges the differential logic circuit).

Regarding claim 11, Morzano shows a wave dynamic differential logic, comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs DI and DI*), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs N1 and P1), and a master-slave differential dynamic logic register configured to transmit on a pre-discharge wave to pre-discharge said differential logic cell (register comprises first stage comprising 38 and 39 and secondary stage 40 and 42, EN signal precharges and predischarges the differential logic circuit).

Regarding claim 12, Morzano shows a wave dynamic differential logic, comprising a differential logic cell having inverted inputs and corresponding non-inverted inputs (inputs DI and DI*), said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs (outputs N1 and P1), and a differential dynamic logic register configured to generate a pre-discharge wave to pre-discharge said differential logic cell (EN signal precharges and predischarges the differential logic circuit).

Regarding claim 23, Morzano shows positive logic (n-type transistors).

Regarding claim 24, Morzano shows positive logic (n-type transistors).

Regarding claim 25, Morzano shows positive logic (n-type transistors).

Response to Arguments

Applicant's arguments with respect to claims 3-12 and 23-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW C. TABLER whose telephone number is (571)270-1567. The examiner can normally be reached on Monday through Friday 8:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 277-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. C. T./
Examiner, Art Unit 2819

/Vibol Tan/
Primary Examiner, Art Unit 2819

December 14, 2009